AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A multiple-supply-voltage semiconductor device comprising:

~~a plurality of blocks~~at least one block~~, any or all of which have an independent clock circuit, and operating with~~ receiving a ~~plurality of power~~ variable supply ~~voltages~~voltage, ~~wherein:~~ said at least one block receiving a clock signal; and

at least one ~~a~~ variable delay circuit which provides a ~~an amount of~~ delay in the clock signals received by the at least one block;

wherein the delay changes ~~changing~~ in accordance with a change in the ~~a power~~ supply voltage ~~is~~ provided to the at least one block~~for any or all of clock signals each of which is provided from a clock generator circuit to each of the plurality of blocks~~.

2. (currently amended): The multi-supply-voltage semiconductor device according to claim 1, wherein the variable delay circuit increases the ~~amount of~~ delay as the ~~power~~ supply voltage decreases.

3. (currently amended): A multi-supply-voltage semiconductor device comprising:

~~a plurality of blocks~~at least one block~~, any or all of which have an independent clock circuit, and operating with~~ receiving a ~~plurality of power~~ variable supply ~~voltages~~voltage, ~~wherein:~~said at least one block receiving a clock signal;

a voltage level detector circuit which detects ~~the~~ a voltage level of the ~~power~~ supply voltage~~ and outputs the detected voltage level as a voltage level detect signal is provided~~; and

~~a~~ at least one variable delay circuit which provides ~~changes an amount of~~ a delay in the clock signal received by the at least one block;

wherein the delay changes in accordance with a change in the voltage level ~~detect signal is provided for any or all of clock signals each of which is provided from a clock generator circuit to each of the plurality of blocks~~ detected by the voltage level detector circuit.

4. (withdrawn) A multi-supply-voltage semiconductor device comprising a plurality of blocks, any or all of which have an independent clock circuit, and operating with a plurality of power supply voltages, wherein:

a phase synchronizing circuit for bringing the clock signals in the blocks into phase is provided for any or all of clock signals each of which is provided from a clock generator circuit to each of the plurality of blocks.

5. (withdrawn) The multi-supply-voltage semiconductor device according to claim 4, wherein a variable delay circuit which provides an amount of delay changing in accordance with the power supply voltage to compensate for a change in delay of a level shifter is provided for any or all of the phase synchronizing circuits, the level shifter adjusting a signal level between blocks supplied with different power supply voltages.

6. (currently amended): The multi-supply-voltage semiconductor device according to claim 1, further comprising:

a voltage change detector circuit which detects a change in the ~~power~~ supply voltage; and

a blocking unit that ~~blocks~~ prevents the ~~a~~ clock signal ~~generated by the clock generator circuit~~ from being supplied to ~~each of~~ the at least one block ~~circuits~~ during a period in which the voltage change detector circuit ~~determines that a voltage is changing~~ detects a change in the supply voltage.

7. (currently amended/withdrawn): The multi-supply-voltage semiconductor device according to claim 1, further comprising:

a minimum voltage detector circuit which generates and outputs a power supply control signal which provides control to ~~minimize~~ limit the ~~power~~ supply voltage within a predetermined range ~~in which a normal operation can be performed at a predetermined clock frequency~~; and

a power supply control circuit which controls the ~~power~~ supply voltage in accordance with the power supply control signal.

8. (withdrawn) A multi-supply-voltage semiconductor device comprising a plurality of blocks, any or all of which have an independent clock circuit, and operating with a plurality of power supply voltages, wherein:

a power supply control circuit which controls the power supply voltage in accordance with an operation mode signal indicating the current operation mode is provided; and

a variable delay circuit which changes an amount of delay in accordance with the operation mode signal is provided for any or all of clock signals each of which is provided from a clock generator circuit to each of the plurality of blocks.

9. (withdrawn): The multi-supply-voltage semiconductor device according to claim 8, further comprising:

a mode change detector circuit which, when detecting a change of the operation mode indicated by the operation mode signal, forces and keeps a clock control signal to a predetermined value for a given period of time set by a timer contained in the mode change detector circuit; and

a blocking unit that blocks a clock signal generated by the clock signal generator circuit from being supplied to each of the block circuits while the clock control signal is kept at the predetermined value.

10. (currently amended): The multi-supply-voltage semiconductor device according to claim 2, further comprising:

a voltage change detector circuit which detects a change in the ~~power~~ supply voltage; and

a blocking unit that ~~blocks~~ prevents the ~~a~~ clock signal ~~generated by the clock generator circuit~~ from being supplied to ~~each of~~ the at least one block ~~circuits~~ during a period in which the voltage change detector circuit ~~determines that a voltage is changing~~detects a change in the supply voltage.

11. (currently amended): The multi-supply-voltage semiconductor device according to claim 3, further comprising:

a voltage change detector circuit which detects a change in the ~~power~~ supply voltage; and

a blocking unit that ~~blocks~~ prevents the ~~a~~ clock signal ~~generated by the clock generator circuit~~ from being supplied to ~~each of~~ the at least one block ~~circuits~~ during a period in which the

voltage change detector circuit ~~determines that a voltage is changing~~detects a change in the supply voltage.

12. (withdrawn): The multi-supply-voltage semiconductor device according to claim 4, further comprising:

a voltage change detector circuit which detects a change in the power supply voltage; and

a blocking unit that blocks a clock signal generated by the clock generator circuit from being supplied to each of the block circuits during a period in which the voltage change detector circuit determines that a voltage is changing.

13. (canceled).

14. (currently amended/withdrawn): The multi-supply-voltage semiconductor device according claim 2, further comprising:

a minimum voltage detector circuit which generates and outputs a power supply control signal which provides control to ~~minimize~~ limit the ~~power~~ supply voltage within a predetermined range ~~in which a normal operation can be performed at a predetermined clock frequency~~; and

a power supply control circuit which controls the ~~power~~ supply voltage in accordance with the power supply control signal.

15-17. (canceled).

18. (currently amended): A multiple-supply-voltage semiconductor device according to claim 1, wherein ~~said~~ the at least one variable delay circuit comprises a multistage inverter ~~in which~~ comprising multiple inverters ~~are~~ connected in series.

19. (currently amended): A multiple-supply-voltage semiconductor device according to claim 1, wherein ~~said~~ the at least one variable delay circuit comprises a plurality of stacked inverter stages ~~stacked vertically~~.

20. (previously presented): A multiple-supply-voltage semiconductor device according to claim 6, wherein said voltage change detector circuit comprises:

an analog to digital converter circuit;

a flip-flop circuit;

and a comparator.

21. (currently amended): A multiple-supply-voltage semiconductor device according to claim 20, wherein said comparator compares a first digital information held in said flip-flop circuit with a second digital information ~~outputted~~ output from said analog to digital converter circuit, and ~~determines~~ detects a change in the ~~power~~ supply voltage if said first and second digital information do not match.

22. (currently amended): A multiple-supply-voltage semiconductor device according to claim 3, wherein said voltage level detector circuit comprises a differential amplifier into which the ~~power~~ supply voltage ~~is input~~ and a reference voltage is input.

23. (currently amended): A multiple-supply-voltage semiconductor device according to claim 3, wherein said at least one variable delay circuit comprises a selector and a delay gate, wherein the delay gate delays ~~a~~ the clock signal ~~from said clock generator circuit~~ and the selector outputs to ~~one of~~ the at least one ~~plurality of blocks~~ block either the clock signal ~~generated by the clock generator circuit~~ or the delayed clock signal generated by the delay gate.

24. (previously presented): A multiple-supply-voltage semiconductor device according to claim 23, wherein said delay gate comprises at least one inverter.

25. (currently amended): A multiple-supply-voltage semiconductor device according to claim 3, wherein said at least one variable delay circuit comprises a selector and a plurality of delay gates, wherein each one of said plurality of delay gates provides a different delay to ~~a~~ the clock signal ~~from said clock generator circuit~~ and the selector outputs to ~~one of~~ the ~~plurality of blocks~~ at least one block either the clock signal ~~generated by the clock generator circuit~~ or one of the delayed clock signals generated by the ~~plurality of~~ delay ~~gates~~ gate.

26. (currently amended): A multiple-supply-voltage semiconductor device according to claim 23, wherein ~~each~~ said delay gate comprises at least one inverter.

27. (new): A multiple-supply-voltage semiconductor device according to claim 1, further comprising a plurality of blocks wherein the clock signal received by the at least one block is independent of any clock signal received by any other block.

28. (new): A multiple-supply-voltage semiconductor device according to claim 3, further comprising a plurality of blocks wherein the clock signal received by the at least one block is independent of any clock signal received by any other block.

29. (new): A multiple-supply-voltage semiconductor device according to claim 3, wherein the voltage level detector circuit outputs the detected voltage level as a voltage level detect signal.